



Molded, 25 mil or 50 mil Pitch, Dual-In-Line Thin Film Resistor, Surface Mount Network

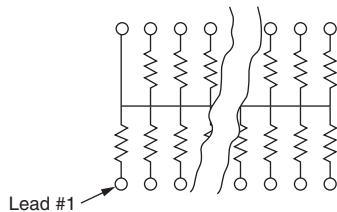


Vishay Dale Thin Film resistor networks are designed to be used in either analog or digital circuits. The use of thin film resistive elements within the network allows you to achieve an infinite number of very low noise and high stability circuits for industrial, medical and scientific instrumentation. Vishay Dale Thin Film resistor networks are packaged in molded plastic packages with sizes that are recognized throughout the world. The rugged packaging offers superior environmental protection and consistent dimensions for ease of placement with automatic SMT equipment. Vishay Dale Thin Film stocks many designs and values for off-the-shelf convenience. With Vishay Dale Thin Film you can depend on quality products delivered on time with service backing the product.

SCHEMATICS

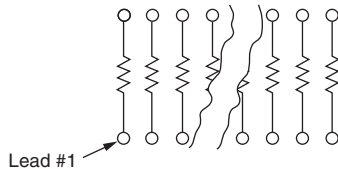
01 SCHEMATIC

Resistance Range:
10 Ω to 47 kΩ

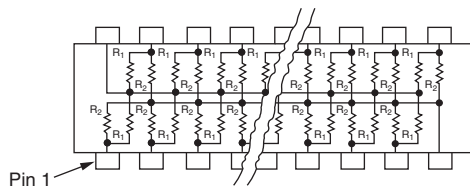


03 SCHEMATIC

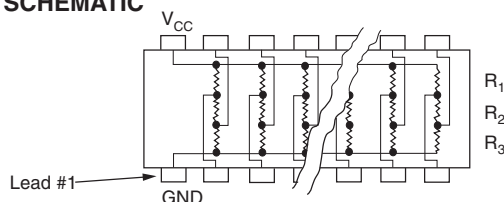
Resistance Range:
10 Ω to 47 kΩ



05 SCHEMATIC



47 SCHEMATIC



FEATURES

- Reduces total assembly costs
- Compatible with automatic surface mounting equipment
- UL 94 V-0 flame resistant
- Thin film tantalum nitride on silicon
- Choice of package sizes: VTSR (TSSOP) JEDEC® MO-153, VSSR (SSOP or QSOP) JEDEC MO-137, VSOR (SOIC narrow) JEDEC MS-012
- Moisture sensitivity level 1 (per IPC/JEDEC STD-20C)
- Isolated/bussed/dual terminator/differential terminator circuits
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS COMPLIANT
HALOGEN FREE

TYPICAL PERFORMANCE

	ABSOLUTE	TRACKING
TCR	100	NA
	ABSOLUTE	RATIO
TOL.	5, 2, 1	NA

RESISTORS WITH ONE PIN COMMON

The 01 circuit provides nominally equal resistors connected between a common pin and a discrete PC board pin.

Commonly used in the following applications:

- MOS/ROM pull-up/-down
- Open collector pull-up
- "Wired OR" pull-up
- Power driven pull-up
- TTL input pull-down
- Digital pulse squaring
- TTL unused gate pull-up
- High speed parallels pull-up

Broad selection of standard values available

ISOLATED RESISTORS

The 03 circuit provides nominally equal resistors isolated from all others and wired directly across.

Commonly used in the following applications:

- "Wired OR" pull-up
- Power driven pull-up
- Powergate pull-up
- Line termination
- Long-line impedance balancing
- LED current limiting
- ECL output pull-down
- TTL input pull-down

Broad selection of standard values available

DUAL-LINE TERMINATOR; PULSE SQUARING

The 05 circuit contains pairs of resistors connected between ground and a common line. The junctions of these resistor pairs are connected to the input leads. The 05 circuits are designed for dual-line termination and pulse squaring.

Standard values are:

VSSR1605:
R₁ = 220 Ω, R₂ = 330 Ω
R₁ = 330 Ω, R₂ = 470 Ω

VSSR2005:
R₁ = 220 Ω, R₂ = 330 Ω
R₁ = 220 Ω, R₂ = 1.8 kΩ
R₁ = 1.5 kΩ, R₂ = 3.3 kΩ

DIFFERENTIAL TERMINATOR

The 47 schematic consists of series resistor sections connected between V_{CC} and ground. Each contains 3 resistors of 2 different resistance values.

Standard values are:

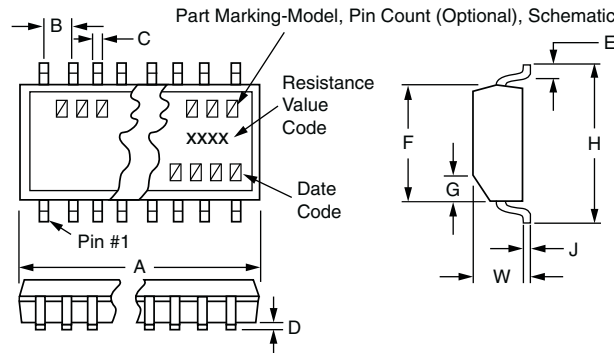
VSSR20 and VTSR20:
R₁ = 270 Ω, R₂ = 120 Ω

VSSR16 and VTSR16:
R₁ = 330 Ω, R₂ = 150 Ω
R₁ = 330 Ω, R₂ = 220 Ω



STANDARD ELECTRICAL SPECIFICATIONS		
TEST	SPECIFICATIONS	CONDITIONS
Material	Tantalum nitride	-
Pin/Lead Number	16, 20, 24	-
Resistance Range	10 Ω to 47 kΩ	Per E-24 table
TCR: Absolute	± 100 ppm/°C	-55 °C to +125 °C
TCR: Tracking	n/a	-
Tolerance: Absolute	± 5 % standard (± 2 % available) ± 1 % standard (check factory)	Per E-24 table Per E-96 table
Tolerance: Ratio	NA	-
Power Rating: Resistor	100 mW max.	At +70 °C
Power Rating: Package	16 = 1.0 W, 20 = 1.2 W, 24 = 1.4 W	0 °C to +70 °C
Stability: Absolute	-	-
Stability: Ratio	-	-
Voltage Coefficient	5 ppm/V (typical)	-
Working Voltage	50 V _{DC}	-
Operating Temperature Range	-55 °C to +125 °C	-
Storage Temperature Range	-55 °C to +150 °C	-
Noise	< -35 dB	-
Thermal EMF	-	-
Shelf Life Stability: Absolute	-	-
Shelf Life Stability: Ratio	-	-

DIMENSIONS AND IMPRINTING in inches (millimeters)



DIMENSION	VTSR-xxxx	VSSR-xxxx	VSOR-xxxx
A - 16 PIN	0.206 ± 0.003 (5.23 ± 0.08)	0.193 ± 0.004 (4.90 ± 0.010)	0.390 ± 0.010 (9.91 ± 0.25)
A - 20 PIN	0.256 ± 0.003 (6.50 ± 0.08)	0.341 ± 0.003 (8.66 ± 0.08)	NA
A - 24 PIN	0.306 ± 0.003 (7.77 ± 0.08)	0.341 ± 0.003 (8.66 ± 0.08)	NA
B (Ref.)	0.0256 (0.65)	0.025 (0.64)	0.050 (1.27)
C (Ref.)	0.0087 (0.22)	0.010 (0.25)	0.016 (0.41)
D	0.004 (0.10)	0.006 (0.15)	0.008 (0.20)
E (Typ.)	0.024 (0.61)	0.025 (0.64)	0.030 (0.76)
F	0.173 ± 0.003 (4.39 ± 0.08)	0.154 ± 0.003 (3.91 ± 0.08)	0.152 ± 0.003 (3.86 ± 0.08)
G	0.015 × 45° (0.38)	0.015 × 45° (0.38)	0.015 × 45° (0.38)
H	0.252 ± 0.005 (6.40 ± 0.13)	0.236 ± 0.008 (5.99 ± 0.20)	0.236 ± 0.005 (5.99 ± 0.13)
J (Ref.)	0.005 (0.13)	0.010 (0.25)	0.008 (0.20)
W	0.043 ± 0.005 (1.09 ± 0.13)	0.064 ± 0.005 (1.63 ± 0.13)	0.064 ± 0.005 (1.63 ± 0.13)

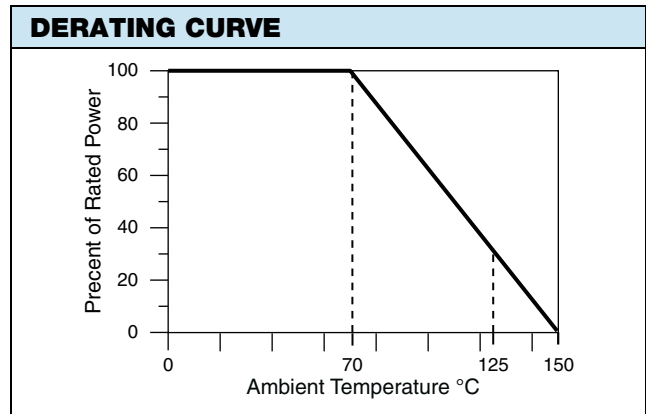
MARKING

MODEL	PIN COUNT (Optional)	SCHEMATIC	RESISTANCE	RESISTANCE	DATE CODE
VXXX	XX	XX	XXXX	XXX	XXXX
VSOR	16	01, 03,	1 % RESISTANCE	OR 1 %, 2 %, 5 % RESISTANCE e.g.: 103 = 10K The first 2 digits are significant figures, the last digit specifies the number of zeros to follow.	
VSSR	20	05 or 47	e.g.: 43R2		
VTSR	24		4 digits are used to express ohmic values only less than 100 Ω. R is used to designate the decimal position		



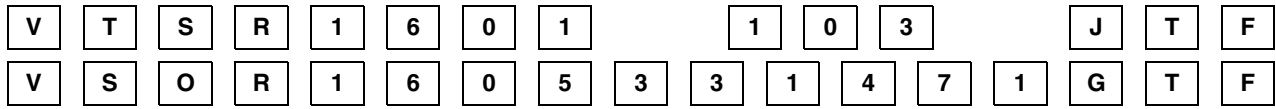
MECHANICAL SPECIFICATIONS	
Resistive Element	Tantalum nitride
Substrate Material	Silicon
Body	Molded epoxy
Terminals	Copper alloy
Plating	100 % matte tin
Lead Coplanarity	0.0005"
Marking Resistance to Solvents	Permanency testing per MIL-STD-202, method 215

PACKAGING INFORMATION			
MODEL	LEADS	TAPE AND REEL	TUBES
VTSR (TSSOP)	16	2500	94
	20	2500	74
	24	2500	62
VSSR (QSOP)	16	2500	98
	20	2500	55
	24	2500	55
VSOR (SOIC)	16	2500	48



GLOBAL PART NUMBER INFORMATION

New Global Part Numbering: **VTSR1601103JTF**



GLOBAL MODEL	PIN COUNT	SCHEMATIC	RESISTANCE (3, 4 or 6 digits)	TOLERANCE	PACKAGING
VTSR VSSR VSOR Lead (Pb)-free (e3) date code > 2705	20 (not VSOR) 24 (not VSOR)	01 (bussed) 03 (isolated)	XXX: ≥ 100R and all 1 %, 2 % and 5 % First 2 digits are significant figures. Last digit specifies number of zeros to follow. XXXX: < 100R 1 % First 3 digits are significant figures. Last digit specifies number of zeros to follow.	F = 1.0 % G = 2.0 % J = 5.0 %	TAPE AND REEL TF = Full reel 2500 UF = Tubed
	16 (not VTSR) 20 (not VSOR)	05 (terminator) 47 (terminator)	xxx xxx First 2 digits are significant figures. Last digit specifies number of zeros.	G = 2.0 % J = 5.0 %	

Historical Part Number example: **VSSR2001102GT/R** (for reference purposes only)

VSSR	20	01	102	G	T/R
MODEL	PIN COUNT	SCHEMATIC	RESISTANCE	TOLERANCE	PACKAGING



Vishay Dale Thin Film Land Patterns

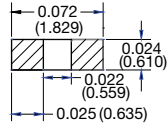
1. Scope

This technical note provides sample land patterns for Vishay Dale Thin Film SMT resistive products. The following drawings are based on IPC-SM-782 Surface Mount Design and Land Pattern Standard. These drawings are for reference only Vishay Thin Film recommends that the user contacts their PC board supplier for actual land patterns required. The pads are intended for lead (Pb)-free and tin / lead solder types.

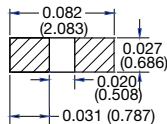
2. Product Series

Thin Film Surface Mount Chip Resistors (FC, L, P, PTN, PLT, PLTT, PLTU, PAT, PATT, PNM, M/D55342 QPL Series)

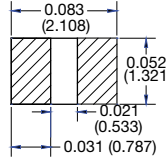
0402 Land Pattern



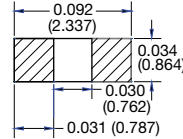
0502 Land Pattern



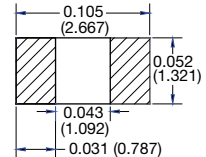
0505 Land Pattern



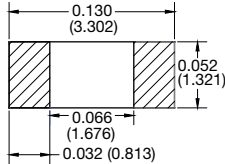
0603 Land Pattern



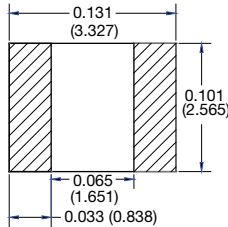
0705 Land Pattern



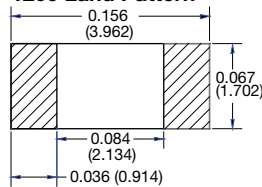
1005 Land Pattern



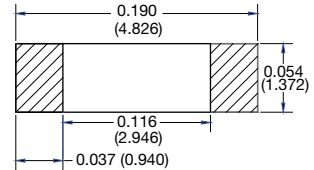
1010 Land Pattern



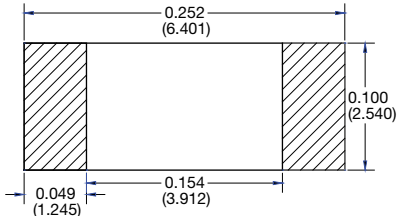
1206 Land Pattern



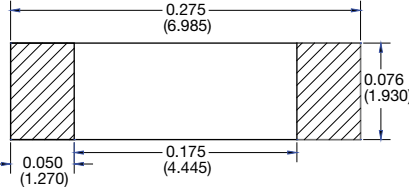
1505 Land Pattern



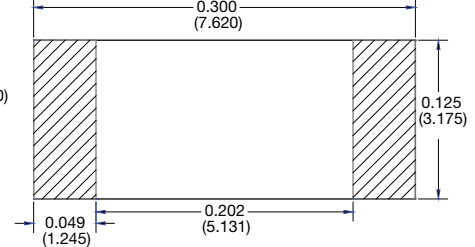
2010 Land Pattern



2208 Land Pattern

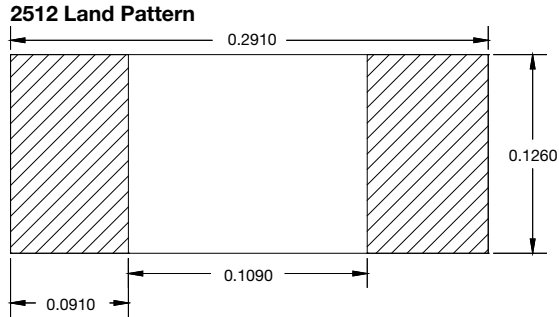
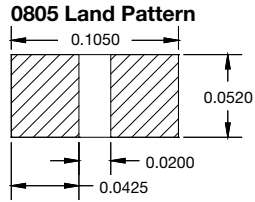
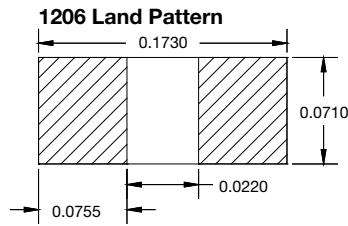
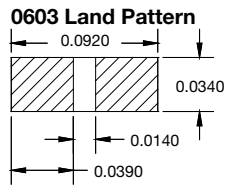


2512 Land Pattern

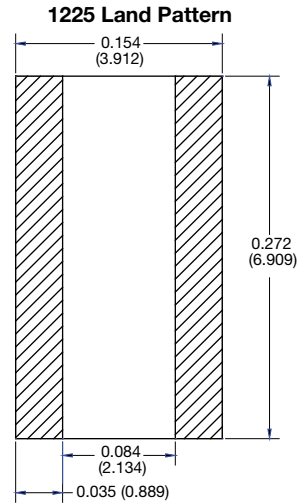
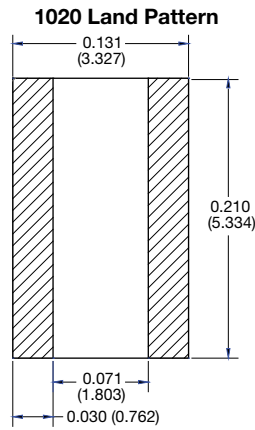
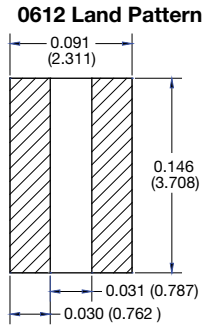
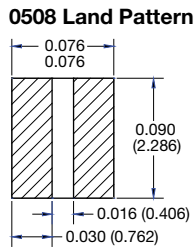




Thin Film Surface Mount Chip Resistors (PHP, PCAN Series)

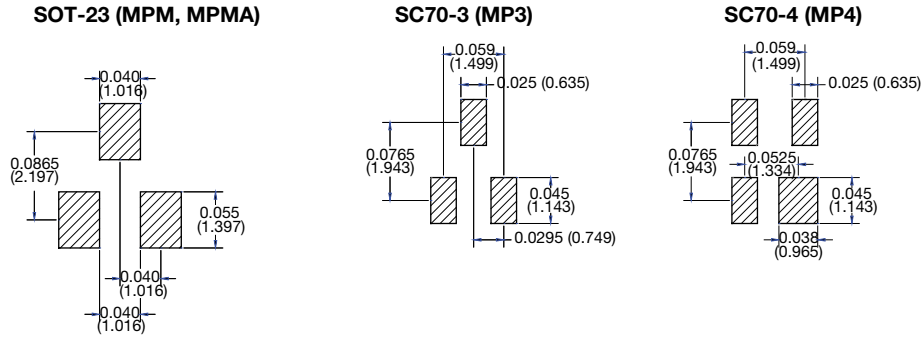


Thin Film Surface Mount Chip Resistors Long Axis Termination (L Series)

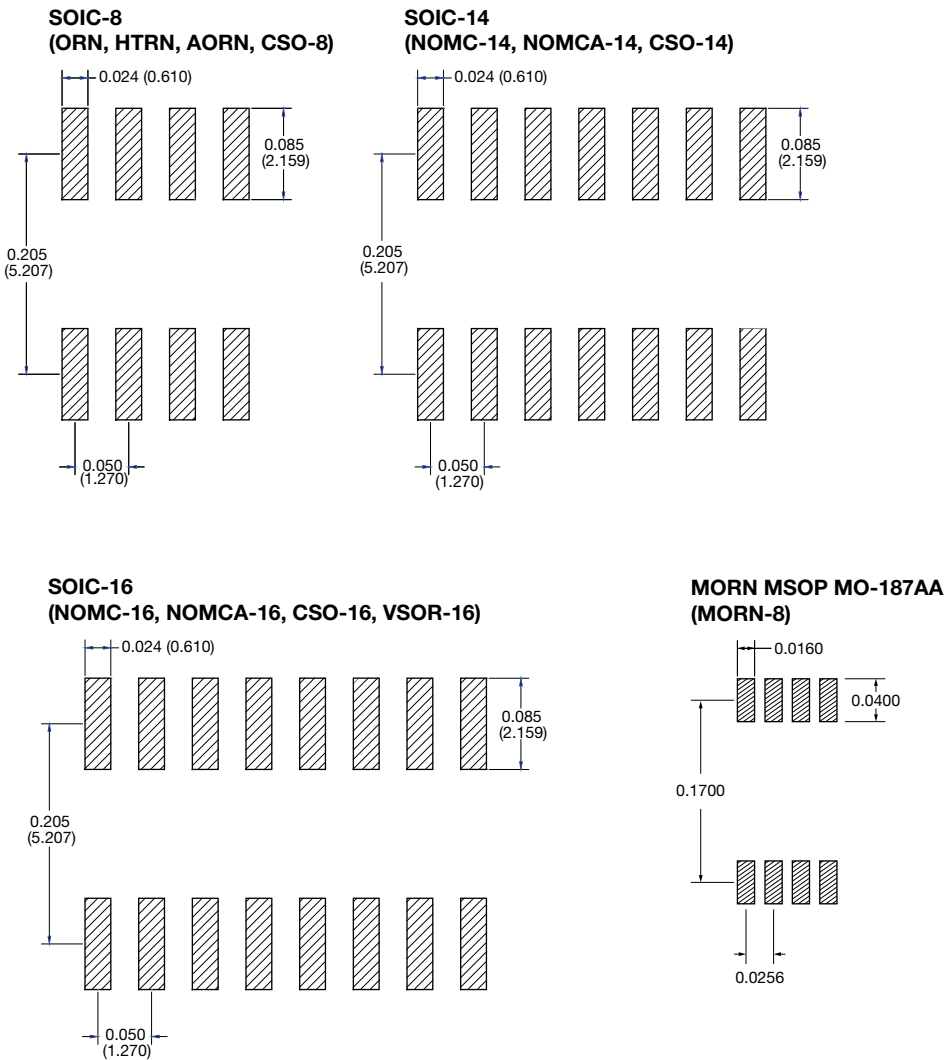




Surface Mount Networks (MPM, MP3, MP4 Series)

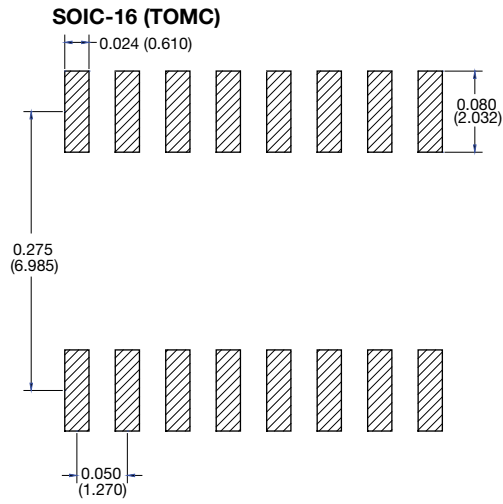


Surface Mount Networks SOIC Narrow Body 150 mils (ORN, CSO, MOMC, HTRN, AORN, MORN Series)

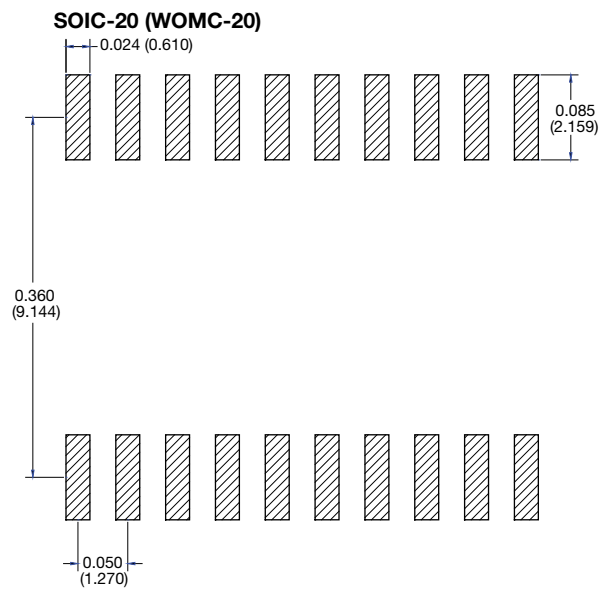
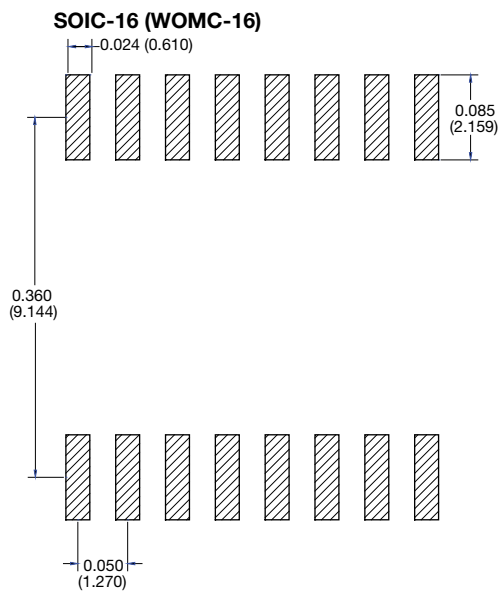




Surface Mount Networks SOIC Medium Body 220 mils (TOMC Series)



Surface Mount Networks SOIC Wide Body 300 mils (WOMC Series)

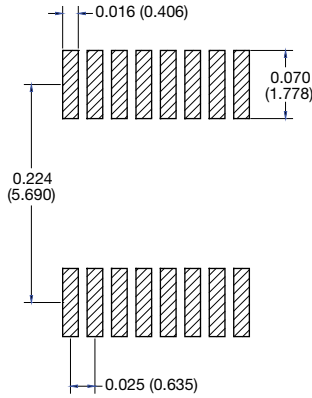




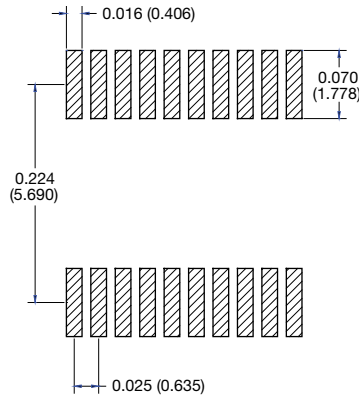
Surface Mount Networks High Density SSOP, TSOP (VSSR, VTSR Series)

SSOP MO-137

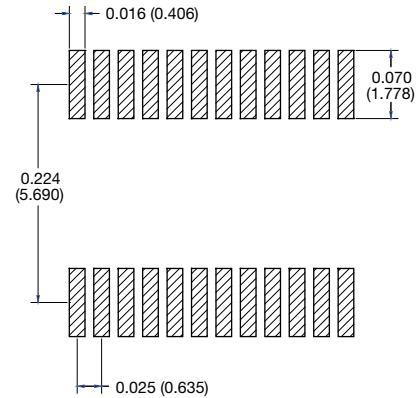
OSOP-16, VSSR-16



OSOP-20, VSSR-20

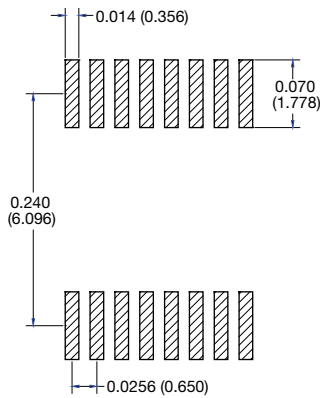


OSOP-24, VSSR-24, HD-CSO-24

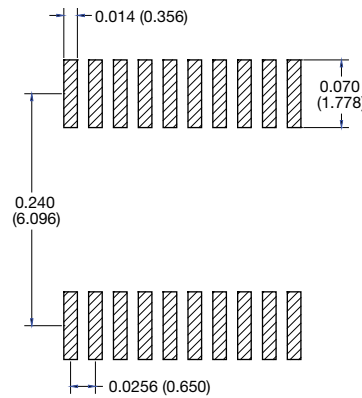


TSSOP MO-153

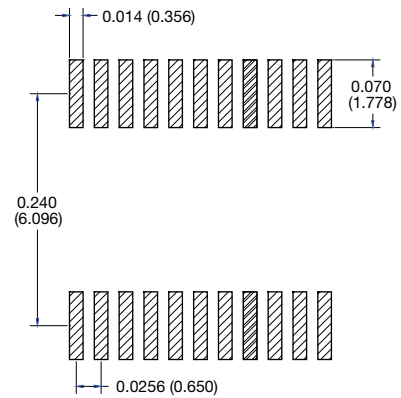
VTSR-16



VTSR-20

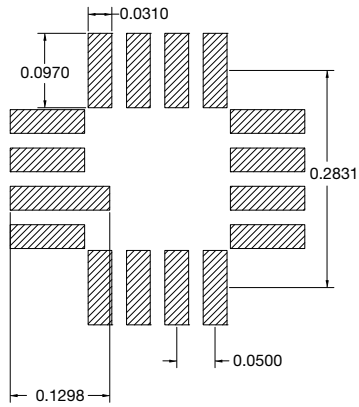


VTSR-24

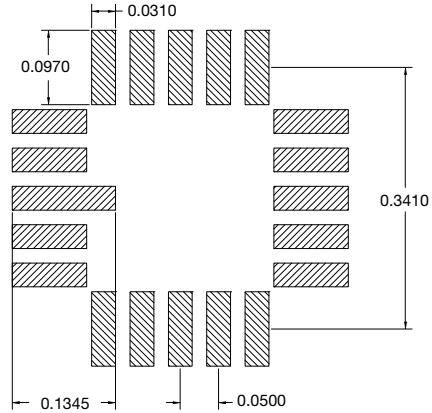


Surface Mount Leadless Networks (LCC Series)

16 Pin LCC

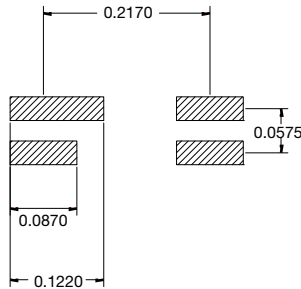


20 Pin LCC



Surface Mount Leadless Networks (MPH Series)

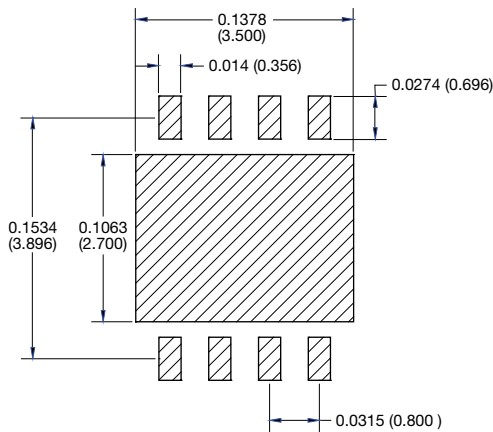
4 Pin LCC



Surface Mount Leadless Packages DUAL/ QUAD Flat No Lead (DFN, QFN Series)

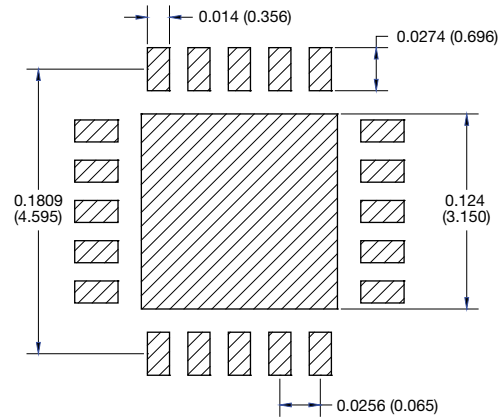
DFN MLP

DFN-8 4 x 5 mm Sq



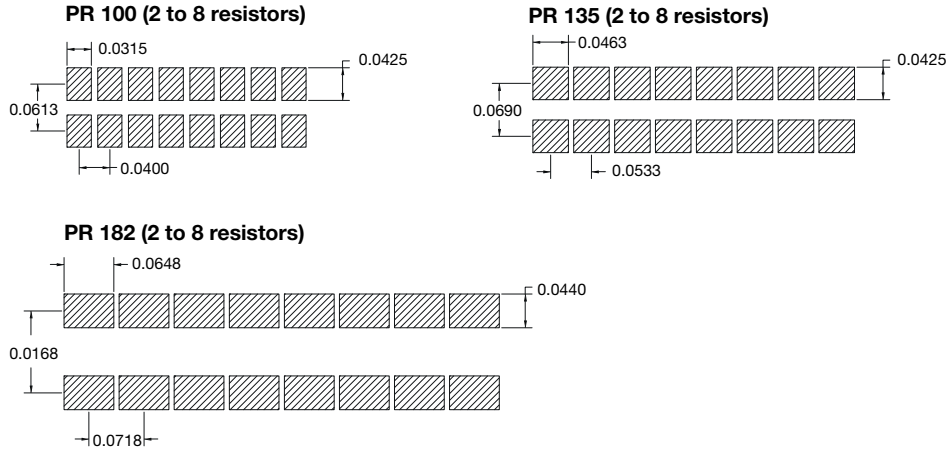
QFN MLP

QFN-20 5 x 5 mm Sq





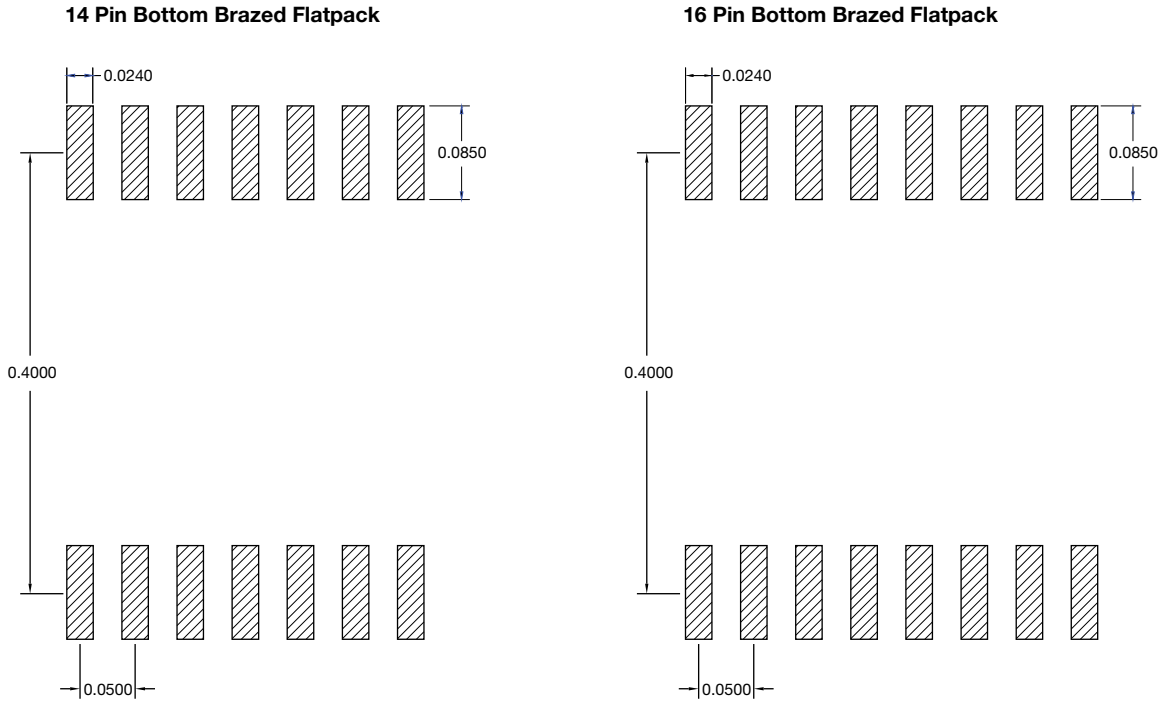
Surface Mount Leadless Resistor Arrays (PR Series)



Note

- All dimensions in inches (mm)

Flatpack





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